**EEE 6742 CAD Tutorial/Assignment #1**

**Total Points:** 26

For the TCL part of the assignment, you should do the following

* Review the TCL resources provided on Canvas to prepare you for future assignments and/or project
* Complete the tasks below to show some mastery of TCL
* Contact the TAs if you have questions

For the rest of the assignment

* You are required to perform a set of tasks using Synopsys Design Compiler – this video may be helpful to you for getting started with Design Compiler (<https://mediasite.video.ufl.edu/Mediasite/Play/7da0e70a6769495a9d3bd820fb8465181d>)
* You can use GUI to learn and get familiar with it, but finally you need to use and submit scripts or testbench files to complete these tasks.
* You need to create a separate report (Tool\_Assignment\_Report.pdf) to answer the questions below.
* You should also include a readme.txt file which contains information about files in the directory and instructions on how to run your script to get the desired output.
* All source code, assignment report file, readme file, tool running log file, and required output files should be zipped and submitted through Canvas.

# **TCL Language**

Write a code in TCL language that *(1 point for each)*

1. Echoes loop number in a for loop
2. Echoes number of files and filenames from a list of files (assume ISCAS85 benchmarks, which can be found online at <http://www.pld.ttu.ee/~maksim/benchmarks/iscas85/verilog/>)
3. Echoes numbers only for each filename from previous task. Find the sum of all the numbers retrieved and echo the result
4. Creates a new folder ‘RTL’ and copy all of files in ISCAS85 to it.
5. Concatenates directory and filenames (and extension if needed)
6. Open and appends filenames with directory in a text file in the for loop. The for loop resonates through the list of filenames.

# **Design Compiler**

Deliverables to submit with the report:

1. A TCL script to synthesize, ungroup and flatten the design s38584.v and output the following information (*10)*
   1. Generates gate level netlist in Verilog format
   2. Reports area, cell, power and timing
   3. Reports constraints (.sdc) and delay file (.sdf)
   4. Reports Fanin cones of g27831 and Fanout cone of g29219
   5. Reports static probability, toggle rate, and switching power for each net
2. Create a “read me” file

Answer the following questions in report:

Q 2.1. What do link library and source library refer to? (*2)*

Q 2.2. What does ‘\_typ’, ‘\_hvt’, ‘\_lvt’ libraries mean? What does the last part mean in the name

“saed32lvt\_ff0p85v125c” for a library? What is the area for an MUX41X2 gate in saed90nm\_typ

library? (*2)*

Q 2.3. Parse the report files to obtain the start point and end point of a critical path. What is the max

delay? (*2)*

Q 2.4. What is the total power consumption? (*2)*

Q 2.5. What is the net load, static probability, toggle rate and switching power for net n6833? (*2)*